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Electrical Silicon Spin Qubits: A Probable Route to Scalability

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Abstract: *Efforts to develop a large-scale quantum computer are being pursued world-wide with the major challenges coming from realization of good quality qubits with high coherence times and also in having scalable device architecture.The engineering problems related to better qubit connectivity and efficient qubit control need also to be simultaneously addressed. Development of quantum dot based silicon spin qubit architecture with an electrical interface for qubit initialization, control and readout seems to be a probable futuristic route to address these challenges and to lead way for possible realization of a practical quantum computer.The paper discusses these two aspects of scalability and engineering of a quantum-classical device interface for the silicon semiconductor spin qubits.*

Key Word*:silicon spin qubits, quantum dots*

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I. Introduction

Quantum mechanics is a branch of physics which explores the working of physical world at the most fundamental atomic and sub-atomic level. Ever since the beginning of the quantum computing paradigm in the 1980s, Richard Feynman[1] and David Duetsch[2] envisioned to harness these unique quantum phenomena for information processing. Quantum computing takes advantage of various quantum phenomena which are fundamentally different from that of classical computing. Quantum computing is a challenge - as the physical world is quantum mechanical, it is a fundamental challenge to utilize the promises and limitations of quantum mechanics for processing of information. Quantum bits or 'qubits' are the fundamental data components of quantum computing. A qubit is essentially a quantum mechanical two-level-system which operates according to one of main the principle of quantum physics - superposition. Unlike an ordinary bit, a qubit can encode a superposition of values i.e. can exist not only in the two states 0 or 1 but also in a linear superposition of these two states with certain probabilities[3]. To build a quantum processor, we first need to form a qubit using a physically addressable pair of quantum levels. The next fundamental requirement is to be able to operate with multiple qubits by way of coupling between the qubits. The final requirement is to have a qubit state measurement capability in a reliable manner without degrading or destroying the quantum information. In order to achieve this, it is necessary to perform the measurements within the qubit coherence time.

The paper first discusses the different qubit fabrication routes. The emphasis is on the suitability of silicon quantum dot based spin qubit architecture which has advantages both in terms of longer coherence times as well as qubit scalability. A practical quantum computer implementation will have millions of such qubits with the requirement of millions of control lines. A large scale classical control infrastructure thus needs to be implemented. However, classical electronics for qubit control have large footprint and operate at room temperature. This makes it difficult to scale up the number of qubits. It will be very useful to develop control electronics with reduced footprint and operational ability at cryogenic temperature to enable faster device operation and scalability. The real challenge is to have reliable qubit control without getting affected by the external environment and loosing coherence. Thiscritical aspect along with the feasibility forrealizing Field Programmable Gate Array (FPGA) based control electronics operable at cryogenic temperature is also discussed briefly.

II. Qubit Implementation Methodologies

The physical implementation of qubits started with the Nuclear Magnetic Resonance (NMR) and Trapped Ion techniques. NMR based qubits use the nuclear spin of atoms within a molecule as the quantum mechanical system. When such a spin is subjected to a strong static magnetic field B_0 it can align or anti-align with this static field, defining the two states 0 or 1. A number of algorithms including Deutsch–Jozsa algorithm[4], Grover's search algorithm[5] and Shor's factoring algorithm[6] have been implemented in NMR. However, these nuclear spins have a low polarization at room temperature making it very difficult to measure the magnetic moment. Scalability of such qubits is also a major concern. These two aspects are the main drawbacks

whenusing NMR technique for quantum computation. Qubits were later implemented using trapped ions. Cirac and Zoller[7] first proposed such implementation in 1995. In that proposal, the qubits were defined as the electron or the nuclear energy states of ions, confined and trapped using appropriate electromagnetic fields. Coulomb interaction forms the basis of coupling the multiple qubits through collective motion of ions in the trap which are controlled using lasers. The inherently long coherence times of ions led to the rapid progress in trapped ion based quantum computing[8]. However, it was realized that scalability is a major issue as the complexity of controlling the ensemble rises with the number of ions squared. So, scalability has remained an outstanding challenge for both NMR and trapped ions-based qubit principle though they have been quite successful in demonstrating good coherence properties.

Solid state approaches for qubit implementation show promise of large-scale integration of a number of qubits along with long coherence times. These qubits fall under 2 majorcategories: superconducting qubits and semiconducting qubits. Under the semiconducting qubits come the Nitrogen-Vacancy (NV) centers in diamond[9-10], implanted phosphorous donors in silicon[11]and electron spin qubits in quantum dots[12-13].

In the year 1999, the first coherent oscillation was observed on charge qubits based on the superconducting principle[14]. Today they are the leading system in solid state quantum computing[15]. These qubits are simply electronic circuits containing lithographically defined Josephson tunnel junctions, capacitors, inductors, and interconnections with the qubit state. These are determined by the number of Cooper pairs which tunnel through the Josephson junction. As the qubit size is relatively large, hence fabrication is relatively easier and not that critical. Therefore, these qubits seem to be one of the strong contenders for the realization of the first quantum computers. The major drawbacks however come in terms of having shorter qubit coherence times, increase in device size and higher power consumption when trying to incorporate billions of such qubits.

Another alternative solid state qubit fabrication route which is recently being pursued worldwide is the semiconductor route. This route encompasses several approaches which include NV (nitrogen-vacancy) centers in diamond, impurity atom doping and the quantum dot based approach. NV fluorescence is dependent on the spin-state because of its energy level structure. The spin state of a NV center can be controlled coherently with the help of resonant microwave fields. NV centers show long spin coherence times even at room temperature because carbon lattice is nearly free of nuclear-spin and has low spin orbit coupling. Apart from this approach, Dr. Kane in 1998[11] also proposed the idea of using dopant phosphorus nuclear spins as the states of a qubit. He proposed to place the dopant phosphorus nucleus in spin-free ^{28}Si by locating two ^{31}P atoms under two adjacent electrodes. Phosphorus nuclear spins were used as qubitswith quantum information stored either in the donor electron, or in the single ^{31}P nuclear spin state, which can be accessed using the electron-nuclear hyperfine coupling[16]. Both these approaches require atomic level precision accuracy to embed donor atoms in a matrix of silicon. They show advantage in terms of longer spin lifetime and thus longer coherence but it is very difficult to precisely dope the donor atoms and connect (or entangle) them in a controlled manner which is of prime importance to perform quantum computations. So both these approaches are not feasible in terms of large scale qubit implementation.

Quantum dot based spin qubits

As an alternate approach to atomic confinement, electrons can be confined as quantum dots (QDs) in a heterostructures i.e. at the interface of two materials having different band gaps. This posed critical requirement in terms of fabrication as we needed to make the quantum dot small enough to show atom like electronic states[17]. So the approach started getting visibility only in the late 1990s, when there were significant improvements in the existing lithographic and nanofabrication techniques. Hayashi et al[18] first reported Quantum dot based coherent oscillations on charge qubits. These charge qubits can achieve high energy splitting. Though this makes it easier to observe the quantum state, but this also makes the qubits more prone to get affected by noise and electrical field. On the other hand, the magnetic moment or the electron spin offers better environmental isolation and is less prone to electric and magnetic field fluctuations. Hence the use of spin qubit states in place of the charged electronic orbital states, offers advantage in terms of longer coherence times. Loss and DiVincenzo[19] were the first to propose this scheme which uses the spin orientations of a single electron trapped in a semiconductor quantum dot, to define the qubit states. Such a quantum dot holding the electron spin was first realized in a GaAs/AlGaAs heterostructures. Negative voltages were applied to gate metal electrodes at the interface which led to the confinement of the quantum dot. Application ofa magnetic field of suitable strength, to this structure resulted in Zeeman splitting of the electron spin states leading to the formation of the required two-level quantum system with the upwards or downwards pointing spin representing the two basis states of the qubit[20].

A major concern with such a device structure was a small resulting coherence time. This was identified to be due to non-zero nuclear spin of all the isotopes of Ga or As which lead to the dephasing of the electron-spin two level structure through hyperfine interactions between the nuclear and electron spins[21]. Hence, Si/SiGe heterostructures to confine the electrons spins in quantum dots was later considered as a more favorable material

in comparison. Nuclear spins are absent in the more-abundant ^{28}Si (~ 96%) isotope and they exhibit a weak spin-orbit coupling, leading to a higher coherence times of few hundred milliseconds. However, the challenge in using Si/SiGe heterostructures was the less developed nanofabrication techniques for Si/SiGe than those used for fabricating the corresponding GaAs based quantum dots. Two new developments in this area helped in overcoming this problem. The first was the use of high-resolution lithography techniques by Eriksson's group, University of Wisconsin and the second was the growth of high-quality heterostructures. These two major developments led to the fabrication of Si/SiGe quantum dot with the capability to be tuned to the few electron regime[22]. Among different proposals for silicon spin qubit implementation[22-23], single electron occupation in a quantum dot was first achieved by Lim et al and Zwanenburg et al in 2009[24-25].

Over the years, microelectronics industry has witnessed exponential progress in silicon and scalability techniques have been well established in the regime of Complementary Metal–Oxide–Semiconductor (CMOS) microelectronics industry. This led to the possibility of electron confinement to 2 dimensions and for creating complex structures to fabricate the desired silicon spins qubits. The gate defined CMOS quantum dot architecturesatisfies the DiVincenzo criteria of scalability, single electron spin initialization, longer coherence time, qubit control (gate operation) and readout. This enables classical computing techniques to make way into quantum devices.

It is thus possible to realize a scalable device architecture using silicon based spin qubits with well defined interactions for large scale quantum computer implementation[26]. For scalability, Si quantum dots having small electrodes (40-50 nm), can be built uniformly into large arrays using lithographic techniques with additional elements such as Quantum Point Contact (QPC) or a Single Electron Transistor (SET) and electron reservoirs built around them. The fabrication process involves trapping single electrons in quantum dots defined electrostatically by surface gates as shown in Fig. 1(a) and (b) in the 2-Dimensional (2D) electron gas at the interface of a Si and SiGe epitaxial layer. The conduction band electrons get accumulated at the interface with their movement restricted only in the lateral direction. On application of negative gate voltage, the 2D electron gas is depleted leading to the formation of quantum dots. Another gate electrode, namely the plunger gate may be used to tune the electrostatic potential of the quantum dot with respect to the reservoirs thus controlling the charge occupancy of the quantum dot.

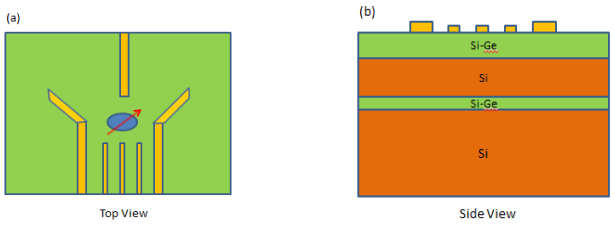

Fig. 1 (a) Spin Quantum dots defined electrostatically by surface gates (b) Si/SiGe heterostructure having 2D electron gas at Si-SiGe interface

Thus the critical requirement for having precise control over the size and charge occupancy of the quantum dot leads to the need to fabricate gate structures with nm sized dimensions by using Electron-beam-lithography. Good reproducibility and device tunability can thus be achieved through this approach. This was recently demonstrated in a linear array of nine dots.[27]

As a further step, a further scaled up device architecture for fabricating a two-dimensional crossbar array of spin qubits was also recently reported in literature[28]. As per the design, three layers are used to define the qubit and the gate structures. The two-dimensional quantum dot array design demonstrates the possibility for having shared qubit control, a scalable number of control lines and high fidelity operation leading way to support implementation of a scalable, universal quantum computer.

III. PERFORMANCE METRICS

In addition to the scalability aspect, a major challenge and fundamental requirement in quantum computing is isolation of the quantum system from its environment. This is essential as the qubit quantum states are extremely prone to perturbation by the environmental fluctuations which consequently disturbs the desired operations of the quantum system. In order to retain the quantum character of the two-level-system (TLS), it is necessary for the qubit toexist as a phase-coherent superposition state and isolation from the surroundings becomes a deciding factor to achieve the desired phase coherence between different possible states[29]. Hence, if the system is not perfectly isolated from its surroundings, the coherence property decays with respect to time resulting in quantum decoherence and gradual loss of quantum behaviour. When choosing a particular quantum TLS for qubit realization, long coherence time therefore becomes one of the most desired criteria.

A lot of progress is being made in realizing gate-based quantum computing device architecture. Certain key properties like the qubit number in a hardware module, effective error rates in single and two-qubit gate operations, qubit coherence and inter qubit connectivity, thus become important to monitor the progress being made in this area. The last few years have witnessed tremendous progress in terms of the mentioned key properties, in the field of silicon spin qubit technology. It is now possible to fabricate multiple spin qubits in array form and exhibiting high single qubit gate fidelities of more than 99.9%.[30] Reasonably good coherence times ranging from 10s of microseconds to milliseconds have been obtained from these qubits and demonstrations of exchange based 2 qubit gates have also been made[31-32]. Hence, it is not hard to envision a computer that would use qubits based on Si technology. One of the leading researchers of the field, Andrea Morello has also quoted, *"Based on what we know now, I do imagine that silicon could become the system of choice at the thousands or millions of qubits level."*

IV. CONTROL AND READOUT ELECTRONICS

For efficient quantum scaling, one prime requirement is the development of a control interface which is able to connect the isolated qubits encoding the quantum information with the classical control and readout technology needed to operate them. Individual addressability of electron spins is also needed incase of silicon quantum dots so that it is possible to manipulate them with voltage-dependent electric fields for scalable device operation and the same has been discussed in some very recent publications[33-35.]

As the number of qubits scales up in future, novel approaches for developing the interface electronics need to be evolved for improved device performance. We need to increase the number and modularity of the independent control channels along with improvement of their performance parameters. Efforts need to be made to decrease the noise and the physical device footprint while increasing the signal bandwidth and the time and amplitude resolution of generated waveforms. Few such technologies to improve the performance of control hardware for silicon CMOS devices have been reported[33].

Along with these aspects, significant improvement in the performance of interface hardware which controls large number of qubits can be achieved if we can embed the control system at cryogenic temperatures[34-35]. This might help in minimization of the signal paths between the quantum and classical interface which may further lead to avoiding timing and synchronization related critical issues. Control electronics architecture implementation of one such system has been done using Field Programmable Gate Array (FPGA) based control electronics, with real time reprogrammable capability even at cryogenics temperatures and is shown in Fig. 2.[35]

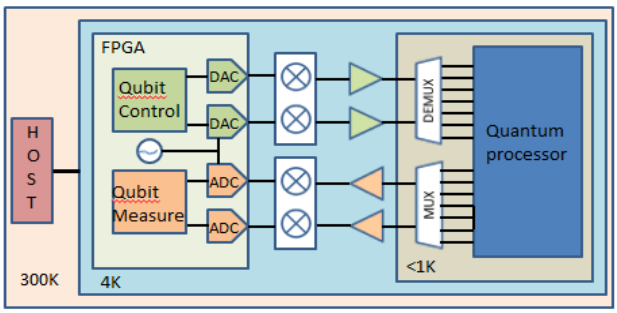

Fig. 2 Cryogenic control platform infrastructure supporting error-correcting micro-architectures

The system reports a time of few 100 ns to carry out qubit read out in a single shot and with nearly 99.9% fidelity. The readout time is limited by various factors. These include the noise of the amplifier and detection systems. The achievable electromagnetic coupling strength between a qubit and the readout circuit also has an effect on the read out time.

The significant point to note however is that many challenges need to be overcome in order to be able to operate an FPGA based board at such cryogenic temperatures, almost 250K below its standard operating range. These include controlling power dissipation and having robust passive components and connectors capable of surviving several cooling cycles without degrading their performance. However, if developed, they can prove to be significant in improving the performance of classical control hardware for developing future quantum technologies.

V. Conclusions

The development of silicon spin qubit technology had a late start in comparison to the two major technologies namely superconducting and trapped ion qubits being widely pursued worldwide. Still, tremendous progress has been made in this technology in the last decade. Based on their performance level, these qubits

have established their suitability and it might be possible that they take a lead for developing future large-scale quantum computers. At present the major hurdle which needs to be overcome is the nanofabrication of these silicon quantum dots and their integration with cryogenic control. Though quite challenging, the same is not unrealistic as shown by the recent advancements in this field.

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